MES COLLEGE OF ENGINEERING KUTTIPURAM

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

One day Workshop on HDL Simulation using Xilinx Vivado

(For the students of Government Women's Polytechnic College Kottakkal)

Date: - 4/3/17 ***Venue: E100- Simulation Lab***

PROGRAM SCHEDULE			
1	Introductory talk	Prof. Mredula L	9.30 a.m
2	Introduction to VLSI design flow	Ms. Ashna A	9.45 -10.30 a.m
3	Tea Break	10.30-10.40 a.m	
4	Introduction to HDL	Ms. Keerthi Vijay	10.40-11.15 a.m
5	Simulation of Digital circuits using Xilinx Vivado	Ms. Sreediya R Ms. Adhin Sali M Ms. Archana C	11.15 a.m -12.30 p.m
6	Lunch Break	12.30-1.30 p.m	
7	Familiarisation Of FPGA	Ms. Shaniba Asmi P	1.30-2.00 p.m
8	Interfacing of FPGA	Ms. Sreediya R Ms. Adhin Sali M Ms. Archana c	2.00-3.20 p.m
9	Tea Break	3.20-3.30 p.m	
10	Concluding Remarks/ Feedback Session/ Certificate distribution	3.30- 3.45 p.m	

HOD